ABSTRACT OF THE DISCLOSURE

A multi-bit vertical memory cell and method of fabricating the same. The multi-bit vertical memory cell comprises a semiconductor substrate with a trench, a plurality of bit lines formed therein near its surface and the bottom trench respectively, a plurality of bit line insulating layers over each bit line, a silicon rich oxide layer conformably formed on the sidewall of the trench and the surface of the surface of the bit line insulating layer, and a word line over the silicon rich oxide layer, and the trench is filled with the word line.